A triggerless data acquisition system for calorimetry - an R&D activity for the Electron Ion Collider (EIC)

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Abstract

We propose to study a triggerless data acquisition system for the EIC Calorimeter, exploring the necessary algorithms to perform an on-line calibration/reconstruction and data filtering on a CPU-server and test the concept on an array of PbWO crystals read by SiPMs. This is one of the leading options for the EIC calorimeter but a triggers scheme can easily be adapted to the other calorimetry technology proposed by the RD1 Calorimeter Consortium. Results will be compared to a traditional FPGA-based data acquisition system. If/when available this system will be tested on other EIC Calorimeter prototypes.

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1) Triggerless data acquisition

To cope with the large data rate and size at detectors front-end, modern experiments use a mix of hardware and software triggers. Usually the first data reduction is achieved by using dedicated boards where a significant filtering is applied by selection algorithms implemented on FPGAs. A CPU farm that reduces the data stream to a manageable size for storing and off-line processing then applies a second, more sophisticated, level of filtering. The main limitations of an FPGA-based trigger reside in: the difficulty of implementing algorithms over a certain degree of complexity and sophistication; the difficulty of optimize the selection criteria reprogramming the boards based on changed requirements; the partial information accessible at front-end level both in the term of quality (usually it incorporates only basic calibration) and quantity (trigger is usually performed using a limited subset of the full detector). These limitations may directly affect the ultimate detector performance and the quality of recorded data since only partial information is available at trigger level, when the decision whether to write or not an event to tape has to be taken. In particular, for an EM calorimeter, an FPGA-based trigger system would have limited capability in identifying EM clusters since not all corrections and calibrations applied in the off-line analysis, can be actually implemented on-line. As a consequence, the on-line time and energy resolution (e.g. the constant term) affecting the event selection is degraded. Another drawback of this approach consists in the impossibility of changing the FPGA-board in case of unexpected experimental configuration changes or upgrades requiring more trigger resources[1].

All these issues are largely solved by moving to a full (CPU) software-based trigger. Thanks to the improved performance of CPU and computer networks, the FPGA-based trigger will be soon replaced by a fully triggerless approach that, removing the hardware trigger and performing the full on-line data reconstruction, provides precise selections of (complicated) final states for further high level physics analysis (see for example the current effort in preparation of the high luminosity upgrade of LHC).

In a triggerless data acquisition scheme, each channel over a threshold implemented on the front-end electronics (or a minimal set of channels), is transferred after being labeled with a time-stamp, disregarding the status of the other channels. A powerful station of CPUs (usually an on-line farm), connected by a fast network link (usually by optical fiber) to the front-end electronic receives all data samples, reorganizes the information ordering hits by time, includes calibration constants, and, at the end, applies algorithms to find specific correlations between reconstructed hits (software trigger), keeping and storing only filtered events. Advantages of this scheme rely in: making use of fully reconstructed (and corrected) hits to define a high-level trigger condition; software trigger implementation in a high-level programming language; easily reprogramming to upgrade the trigger configuration and accommodate new requirements dictated by changed triggering conditions. Furthermore, the system can be scaled to match different experimental conditions (unexpected or foreseen in a planned upgrade) by simply adding more computing (CPUs) and/or data transfer (network switches) resources.

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[1] The JLab-HPS experiment had a similar issue when, due to the high rate induced by the beam background, some of the channels of the PBWO calorimeter had to be removed from the trigger reducing the detector acceptance.

2) A triggerless DAQ for EIC

These considerations apply to the electromagnetic calorimeter of the future Electron Ion Collider (EIC), independently on the technology that will be chosen (crystals, powder/scintillators, Shashlik, ...) and, largely, independently on the photo-sensors will be used (SiPMs, APDs, PMTs ...). The EMCAL will be one of the key elements defining the trigger for most, if not all the processes of interest for the realization of the EIC physics program since it will be crucial for tagging the scattered electron. For this reason, we propose the study and development of a triggerless data acquisition system optimized for the EMCAL readout.

A triggerless option may result in: on-line implementation of calibration constants to compensate for longitudinal and transverse EM shower leakage and gain variation, providing a more precise reconstruction of the energy deposition (and therefore an improvement in the ultimate energy resolution); implementation of more sophisticated clustering algorithms for a better reconstruction of close-by tracks allowing to resolve gammas from π^0 in a wider kinematics; improvement in EM/hadron shower discrimination for a more efficient pion rejection.

A triggerless DAQ provides significant advantages for all reaction channels will be studied in EIC (independently on its implementation at BNL or JLab). In the following we briefly describe the trigger requirements of the main channels highlighting the pros of a triggerless option.

- **InclusiveDIS**: the scattered electron detection requires an excellent discrimination against hadrons and photons. Assuming a 5 GeV x 50 GeV configuration, for $\eta > -2$, electrons with $p<5$GeV/c are overwhelmed by background from hadro-production. The triggerless algorithm can be programmed to better distinguish between the EM shower produced by the electron and the hadronic shower due to energetic mesons as well as MIPs signature. A single cluster vs multiple-clusters and the determination of the total energy accumulated in the shower will provide a mean to reduce neutral background (mainly gammas form π^0 decay) providing a significant increase in the lepton trigger purity.

- **Semi-inclusiveDIS**: the same arguments reported above apply to SIDIS too. The capability of identifing hadrons with high efficiency at the trigger level provides an efficient quark flavour tagging. A combination of calorimeter information together with the PiD provided by the other detector components, such as the RICH, will provide robust selection criteria. Events with electron + 1h, electron + 2h, ..., electron + Nh will be optimised to select mesons and baryons in the final state.

- **Exclusive**: this is the most challenging and demanding conditions for the EIC trigger. A good electron/hadron discrimination in a wide rapidity interval, the capability of distinguish single-from multi-cluster events, the separation of EM clusters from background down to 1 GeV momentum and the capability of particle multiplicity counting, require sophisticated algorithms difficult to be implemented in an FPGA-based trigger scheme. A triggerless option where several trigger conditions can be programmed and implemented using high-level languages provides a unique advantage. Detailed studies show, for instance, that the DVCS physics program will strongly benefit by the measurement of the hard photon in conjunction with the electron identification. The dominant Bethe-Heitler

background will be selected and rejected by identifying the polar angles of electron and gamma and applying a tight $(\theta e - \theta\gamma) > 0$ cut. Access to largely reconstructed observables (that include detector calibration for a better accuracy) as well as the application of complicated cuts in the kinematics domain become easy in a triggerless scheme where reconstruction and selection algorithms can run on-line on a CPU farm.

Just for completeness, we would like to mention that a triggerless scheme will facilitate future extensions of the envisaged EIC physics program. For instance, if hadron spectroscopy will complement the rich physics program of the EIC, multi-hadrons production triggers tailored on rare finals states difficult to access experimentally (e.g. kaon-rich reactions) would require to set and add multiple and sophisticated algorithms to select the physics of interest. Same rational is valid for other physics program will be considered in the future.

Despite the conceptual simplicity of a triggerless DAQ, a realistic implementation with the specific detector readout is necessary to demonstrate the expected performance. The sophisticated combination of a suitable front-end electronics, network facilities and CPU algorithms require a significant effort to identify, or develop in case they are not yet available, the best option for each element, set-up and test the whole scheme and compare results with more traditional approaches. For these reasons, a dedicated R&D program should start soon to explore the practical implementation for the EIC calorimeter readout as well as quantify the effectiveness and the efficiency of this option when compared to the traditional FPGA-based trigger system. In particular, by removing any bias (thresholds, cuts, ...) introduced by FPGA-based trigger systems, it will be possible to study the trigger effect on the ultimate detector resolution and check whether it matches the EIC physics program requirements. Based on the results of this R&D activity, this scheme could then be extended to other EIC detectors, setting the ground for broader program in the next years.

In the following we will focus on a specific photo-readout based on SiPMs, since we believe that this rapidly growing technology will lead the readout options in the future but, as mentioned above, a similar scheme will also work in case different photo-sensors will be chosen.

3) A triggerless SiPM matrix readout

We propose to explore the use of a triggerless data acquisition for a SiPM-instrumented matrix of EIC ECal channels. The proposed activity includes:

- implementation of a 16ch DAQ system based on a commercial fADC that allows for triggerless readout;
- implementation of the full SiPM operation and read-out chain based on discrete components, including: the HV-power supply, the analog front-end to match the requested digitiser input; the signal digitisation and triggerless read-out;
- development and test of trigger algorithms to be implemented on a on-line farm of CPUs;
- performance comparison with results obtained using a traditional FPGA-based trigger DAQ;

The concept will be validated by running preliminary tests on an array of 2x2 PbWO crystals instrumented with SiPM. The crystals are available and ready to be assembled in a matrix. PbWO represents a leading choice for the EIC calorimeters and results of this R&D will be particularly significant to validate the proposed technology in a realistic configuration. Thanks to the high-level programming of the software trigger, it will be easy to adapt the selection criteria to different crystals/configurations for the optimization of the other EM calorimeter options. If the sub-proposal "High density (80W20Cu) shashlik with improved performance" will be approved as part of this Consortium, we will test the triggerless DAQ system on a SiPM readout small-scale prototype, as soon as ready for beam testing. The prototype will provide a second realistic case study for a triggerless EIC DAQ system, mimicking the central tower of an EIC Shashlik calorimeter. The peripheral channels of each Shashlik module, instead, have less stringent digitization requirements, hence an ASIC-based readout, still based on a triggerless scheme, may be more suitable. On a longer timescale, we thus envisage a possible continuation of the R&D activity focused on the development of online algorithms to synchronize and correlate all the channels in one module, where different FEE systems are used[2].

The proposed activity fits in the one-year timeline imposed by the EIC R&D but we can envisage a follow-up of this activity. Based on the obtained results, we consider developing a new DAQ board that incorporates the front-end chain in a single PCB (SiPM power supply, analog front-end, digitization) linked to the CPU-based read-out with a fast-synchronized ethernet connection (e.g. White Rabbit system). This would represent the basic element of a full calorimeter data acquisition system.

4) Proposed R&D activity

The proposed R&D activity is composed by 3 tasks: study of the triggerless readout, comparison to an FPGA-based trigger option, and, based on obtained results, development of an optimize board matched to the EIC calorimeter specifications.

I) Study of the triggerless readout

The first task of the project consists in setting up a full front-end/read-out/software-trigger chain for a SiPM array prototype:

- instrument the 2x2 PbWO crystal array with SiPMs. We will use the Hamamatsu 13360-6075, 6x6 mm^2 in active area with cell-size of 75 μm to cover the larger area and avoid saturation issues at large energy; If necessary, both sides of the crystal will be instrumented for dual read-out.
- Develop the necessary front-end electronics (preamplifier, bias voltage supply) to interface with the fADC board;

[2] As discussed before, by "triggerless" system we mean a general TDAQ architecture where each detector channel (or group of channels) is read by front-end electronics (FEE), that continuously sends a stream of hits to the online CPU farm. A "hit" is created whenever a "local trigger condition" is satisfied, in the simplest case, when the signal seen by the FEE crosses a programmable threshold. Among other data contained in the "hit" (depending on detector details), a timestamp must be included to properly order and match hits from different channels and subdetectors.

• develop algorithms for the CAEN digitizer V1725 (14-bit, 250Ms/s, 16ch) to download data when a channel-overthreshold is found, via the optical link to the CPU-server;

• develop the data acquisition program to read the data stream from the board, perform calibration/correction and transfer the cooked data to the internal memory for further processing;

• design an EventBuilder that, using the event time stamp and the geometry information on the crystal position, aggregates the time-correlated single channel hits in an event providing high level information: time, energy and particle identification;

• develop a GEANT4 model of the array to study the response of the crystals to different particles: electron/gamma (EM shower), muons (MIPs and cosmic rays), pions/protons (hadronic shower);

• explore and study algorithms to define trigger conditions corresponding to different event topologies (EM shower, hadronic shower, cosmic rays, ...) based on GEANT4 simulation of the array response; optimize chosen algorithms to maximize the effciency for identifying the events of interest and minimize any possible bias induced by the selection conditions;

• develop data transfer protocol and disk storing with an optimized data-compression to keep the event-size limited..

This set-up, limited to a single front-end board (max 16ch), represents the basic unit of a multi-channel triggerless DAQ. Multi-boards connection requires a more sophisticated data transfer scheme based on advanced network systems (e.g. White Rabbit) able to maintain the synchronization between the front-end boards and the CPU-server. Other experiments are developing similar read-out schemes for multi-boards front-end electronics (e.g. KM-3-NET Collaboration) that could be tested in a follow-up of this project.

II) Comparison to an FPGA-based trigger readout

The second task of the project consists in testing the same experimental set up instrumented with a traditional FPGA-based trigger and compare results to what obtained with the triggerless option:

• replace the CAEN board with the fADC250 (12-bit, 250Ms/s, 16 ch) developed by Jefferson Lab that uses the VME-VXS backplane to transfer data to a Read-Out-Controller (ROC) in the crate Ethernet-connected to the DAQ server;

• implement some simple trigger algorithms (cluster, cosmic ray, MIPs) in the FPGA hosted by the Crate Trigger Processor (CTP) placed in the VME-VXS crate;

• install and test CODA2.0 (Cebaf Online Data Acquisition) to collect data and write on disk;

• off-line, correct data implementing calibration constants and correction and develop en EventBuilder that provide the event information: time, energy and particle Id;

• compare performance and results obtained with triggerless and FPGA-trigger DAQ.

III) An optimize board for triggerless readout

The last task of the project consists in designing a board that integrates the discrete components tested during the previous activity:

• study a modular design to adapt the board to different photo-sensor readouts (SiPM, APD, PMT) by implementing the analog front-end and power distribution on mezzanines;

• define the specifications of variuos modules (using SiPM-based read-out as leading option): power supply, analog front-end, digitisation, filtering, data aggregation, data transfer;

• design the block diagram of the board.

The realisation of the electric diagram and the PCB implementation of the board are left to a possible renewal of this R&D activity. This will also include the realisation of a prototype and tests with the same array of crystals described above.

5) Timeschedule, milestones, deliverables and funding requests

The time schedule for the proposed R&D activity is reported in Tab.1. At the end of the 1-year R&D term we expect to have tested the full triggerless DAQ chain on a 2x2 PbWO crystals array and compared with the traditional FPGA trigger DAQ. This will represent the first step towards a comprehensive test of a triggerless DAQ system for the EIC Calorimeter. Two milestones, set in the middle and at the end of the 1-year term, allow the project reviewer to check progress of the project.
After the first six months, a report documenting the setup and commissioning of the DAQ system and detector will be made available. At the end of the 1-year term, the proposed R&D activity will produce a detailed report describing the achievements obtained with the triggerless readout, results of the comparison with the FPGA-based DAQ and the block diagram of the custom board that will be used as a starting point for the continuation of this activity in a second year term. Table 2 summaries the list of deliverables.
If funded for another term, the follow-up of this activity will include: the on-beam tests of one or more prototypes developed by other consortium members (e.g. the Shashlik prototype), the realisation of a triggerless modular acquisition board optimised for SiPM readout, and the development of the network infrastructure necessary to fully exploit the potentialities of this technology.

To achieve the proposed R&D program, we are mainly accounting on instrumentation and equipment funded by INFN. Many components are already available (crystals array, VME-VXS crate, HV power supply, ...) and part will be bought with available funds (SIPMs, analogic preamplifiers, a powerful CPU-server to run the triggerless DAQ, high performance network switch, ...). The total value of matching funds can be estimated in ~ $50k. We request funds to procure the CAEN V1725 ($10k) digitiser and consumables ($2k). In addition a minimal provision for travel funds ($6k) is requested to partially cover expenses for implementation of the FPGA-based trigger readout that will be done with JLab experts support. We have chosen the CAEN V1725 (16 channels, 14-bits, 250 MHz, optical readout, single-channel trigger capability) since it represents the optimal match between costs and

performance (a large dynamic range at reasonably fast sampling rate), providing the necessary flexibility to cope with different photo-sensor technologies (SiPM, APD, PMTs). The 16 channels would allow us to extend tests to larger size EIC calorimeter prototypes if/when needed. In case of reduced budget (20% cut scenario) we may consider the option of a less recent CAEN digitiser, e.g. the 8 channels, 12-bits, 250 Ms/s V1720 that, for a reduced cost, will allow us to set up the triggerless readout of the 2x2 PbWO crystals array. The limited dynamics (12-bits vs 14-bits) and the reduced number of channels (8 vs 16) will reduce the sensitivity to the ultimate performance of the system, requiring to procure another module in case we will extend the readout to a larger prototype.

In term of personnel, the R&D program will be conducted mainly by INFN staff scientists and technicians (listed at the beginning of this document), and will benefit of the support of the INFN-Genova Electronic and Computing Service. In particular, the design of the custom triggerless readout board will be responsibility of INFN Electronic service. We are requesting funds to hire a dedicated post-doc for 1-year. The young researcher will work together and supervised by the PIs of this proposal, conducting his activity at INFN-Genova (Italy) and Jefferson Lab. His/her primary responsibility will be the study and development of the algorithms for triggerless readout and the experimental measurements. We are aware that this grant can not guarantee a standard 2-years post-doc position but, given the presented program, in case a second 1-year term will not be funded, we are confident that INFN will supply the matching funds providing the continuation of the proposed R&D program.

The quantization of a 1-year post-doc fellowship prevents the definition of 40% cut scenario for the proposed R&D program. Table 3 summaries the funding request.

Table 1: 1-year time schedule for proposed tasks/subtasks.

TASKS/Subtasks	Q1	Q2	Q3	Q4
Test bed and detector set-up implementation				
Triggerless system procurement and set-up: CAEN V1725, analog front-end, SIPM power supply	X			
FPGA-based trigger procurement and set-up: VME-VXS crate, VTP, ROC, JLab fADC	X			
Assembly and deployment of a 2x2 PbWO crystals array	X	X		
MILESTONE M1: DAQ systems and detector ready for tests		M1		
Trigger algorithms implementation and comparison				
Read-out and EventBuilder implementation (both systems)	X	X	X	
Development of trigger algorithms on CPU	X	X	X	
Development of trigger algorithms on FPGA	X	X	X	X
MILESTONE M2: comparison of results obtained with a CPU-and FPGA-based DAQ				M2
Preliminary design of triggerless custom board				
Development of a modular design and specification definition of the triggerless board	X	X	X	X
MILESTONE M3: Block diagram of custom triggerless board				M3

Table 2: Deliverables.

Deliverable	Due date
Commissioning of test set up (DAQ and detector)	end of Q2
Triggerless readout activity report and triggerless board block diagram	end of Q4

Table 3: Funding request.

Equipment: CAEN V1725 14-bit, 250Ms/s, fADC + ancillary components	$10k
Consumables: cables, connectors, interfaces	$2k
Travel funds for visits at JLab and other contacts	$6k
Personnel: 1-year post-doc position	$40k
Total	$58k